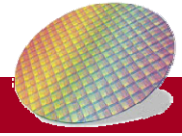
Computer Organization



Course Administration

- Instructor: Ing-Chao Lin (林英超)
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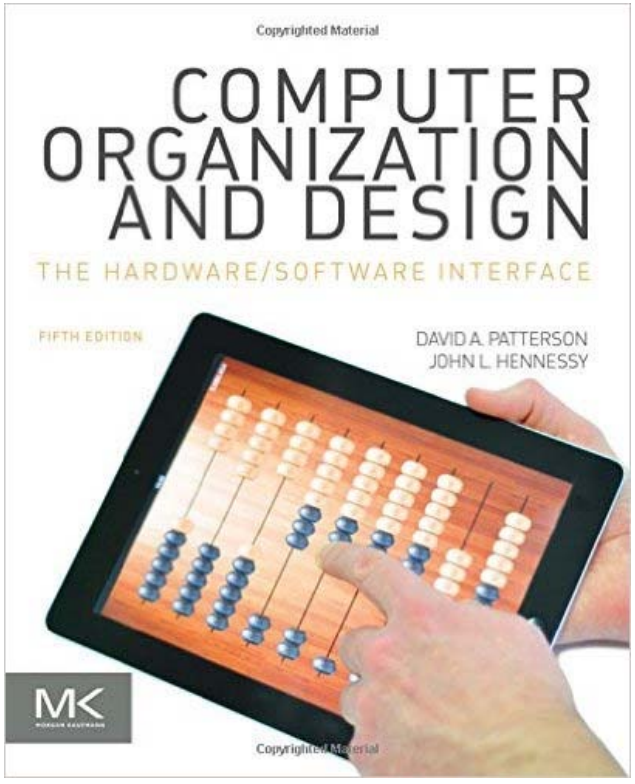
  - Tel: +8866-2757575 ext. 62553
- Teaching Assistant: TBD
  - Lab:
    - Phone: 06-2757575 ext. 62530-33
    - Email: nckuco@gmail.com
- Course Website:
  - http://www.caid.tw/home/courses/comporg/comporg2017
    - announces and slides will be posted here
  - http://moodle.ncku.edu.tw – submit your homework there

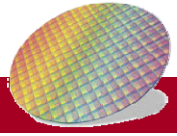
Textbook

- Textbook
  - Computer Organization and Design: The Hardware/Software Interface, fifth ed. by David Patterson and John Hennessy



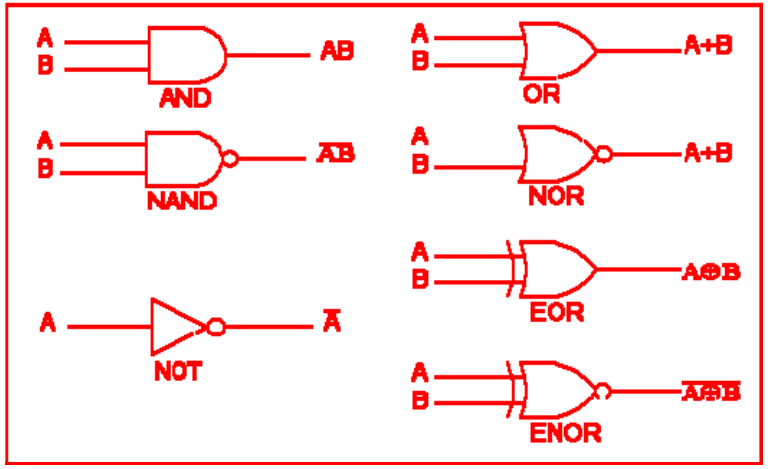
Topics Covered

- Verilog
- Computer Abstraction and Technology
  - Components of computers
  - Performance
  - Power
- Instructions
  - MIPS instruction format
- Arithmetic for Computers
  - Addition/Subtraction
  - Multiplication/ Floating point
- The Processor
  - Data path /pipeline
- Memory Hierarchy
  - Cache basics/ Virtual memory
- Parallel Processors from Client to Cloud

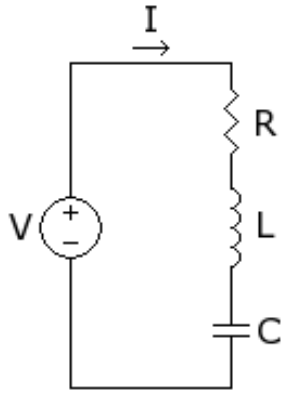


Prerequisite

- Introduction to Circuits Theory and Digital Electronics (F720401)
  - Basic Circuit Theory
  - Frequency response and Bode plot
  - Semiconductor and Transistors
  - Transistor Circuitry and Amplifier
  - Logic Circuits



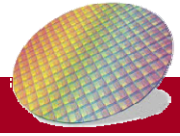
- Introduction to Digital System (F720900)
  - Logic Gates and Gate-Level Minimization
  - Combinational Logic and Synchronous Sequential Logic



- Programming Language: C and Verilog

Tentative Grading

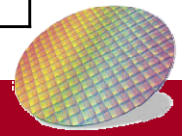
- Homework and Lab Assignment (40 %)
- 3 Exams (45%)
- Class Participation (Attendance and In-class quick test, 15%)
  - You need to sign the attendance sheet in each class
  - If someone else sign for you, you will lose 5 points of your final grade for each violation.
  - Honesty is the best policy.
- Percentage of each part may change



Homework and Lab Assignment

- Homework and Lab Assignment
  - Additional Lab hour on
  - No late submission without justified reasons
  - Grading for each homework
    - Code, Report, Demo : You need to demonstrate and explain your codes to TA. You need you carefully understand your code before talking to TA. If you cannot explain your code clearly, you will lose points

HW& Lab (40%)			3 Exam(45%)	Class Participation (15%)
Code	Report	Demo		
50%	20%	30%		



國立成功大學學則

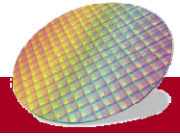
- 第九條 學生因請假而缺課者，稱為缺席，無故缺席者稱為曠課。學生請假辦法另定之。
- 第十條 學生曠課一小時，扣所缺科目學業成績分數一分，請假缺席三小時，扣所缺科目學業成績分數一分。因公請假，或因病請假而經醫生診斷出具證明書，或因懷孕、生產、哺育三歲以下幼兒而核准之事（病）假、產假，其缺席不扣分。
- More rules
  - 國立成功大學試場規則
  - 國立成功大學學生缺席、曠課扣分、扣考辦法
  - 國立成功大學教室使用守則

http://cid.acad.ncku.edu.tw/files/11-1056-603.php

Laptop & Tablet issue

- It's OK if you use your laptop or tablet or phone for class-related issues, such as reading course slides.
- However, It's not allowed to use laptop or tablet for things that are not related to class.
- I want everyone to be here and present

You will lose 2 points of your final grade for each violation.



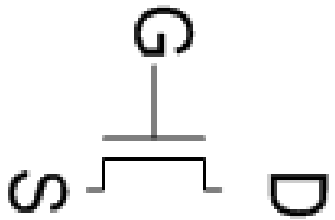
Homework 1 (1% of your final grade)

- Prepare a PowerPoint slide and put your head shot picture (大頭照.
- Submit on Moodle by 3/1 (Wed) 9:50PM.
- Mail to nckuco@gmail.com if the course is not in your moodle.
- See another file for the example

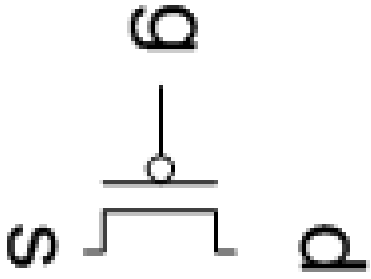
In-class quick test

- In-class quick test is a very simple test.
- Normally take less than 30 minutes.
- Cover what I taught in class
- Basically, it is random, and will not be announced in advance

Recap of basic MOS transistors and logic gates



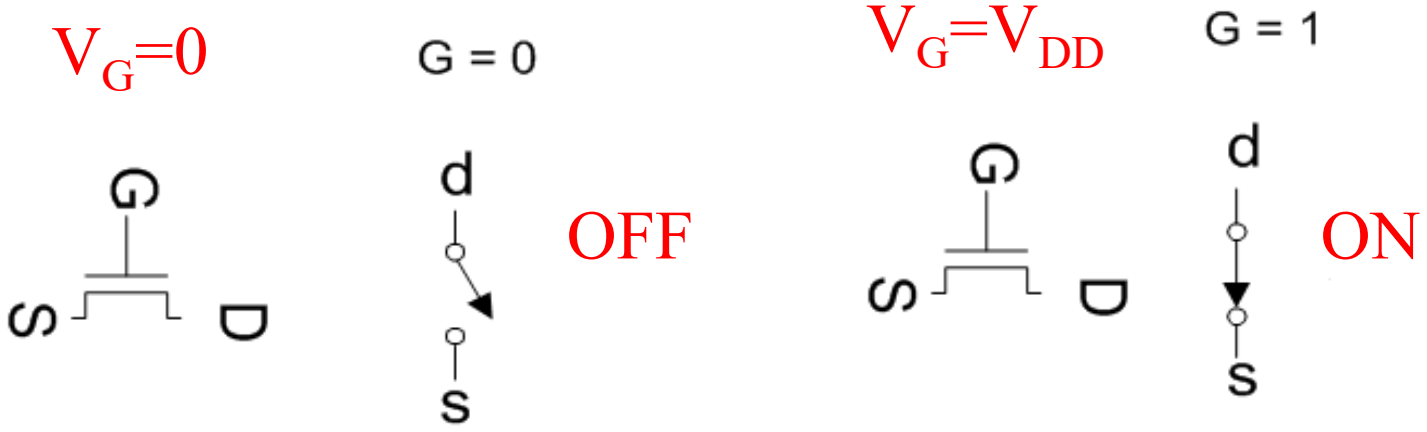
NMOS



PMOS

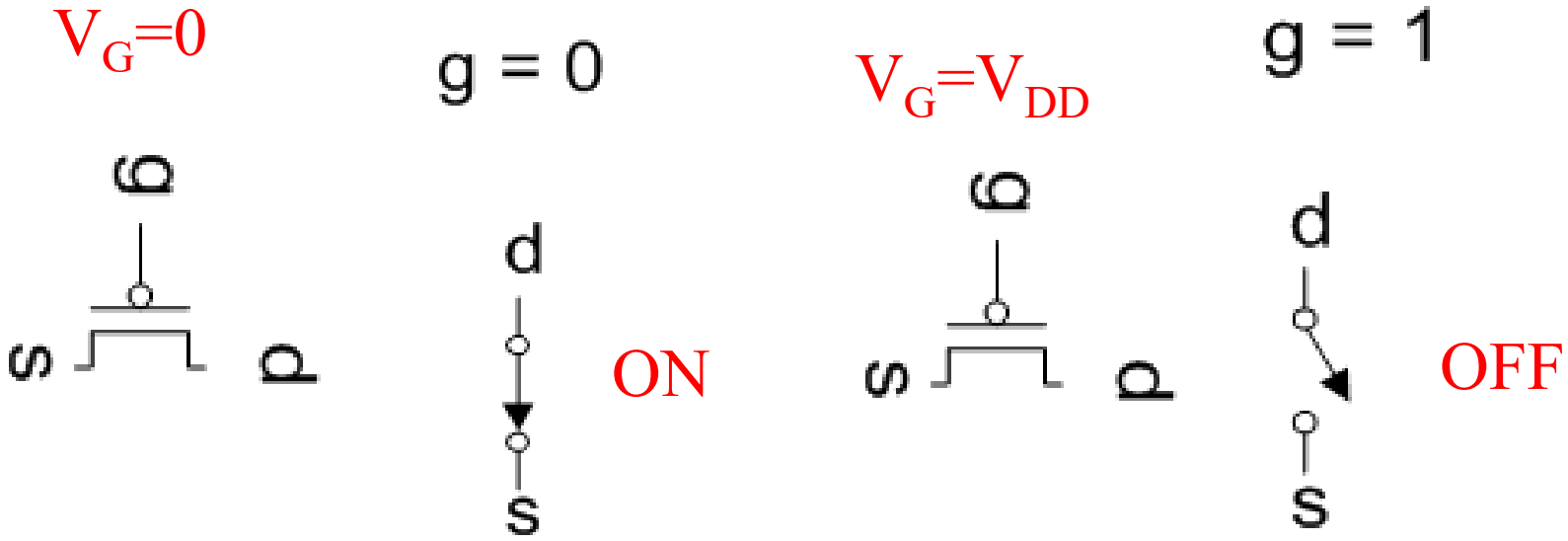
nMOS transistor

- When the gate is at a low voltage (V_G=0):
  - No channel, transistor is off
- When the gate is at a high voltage (V_G=V_{DD}):
  - Positive voltage inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



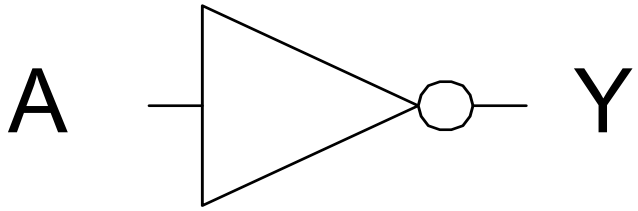
pMOS Transistor

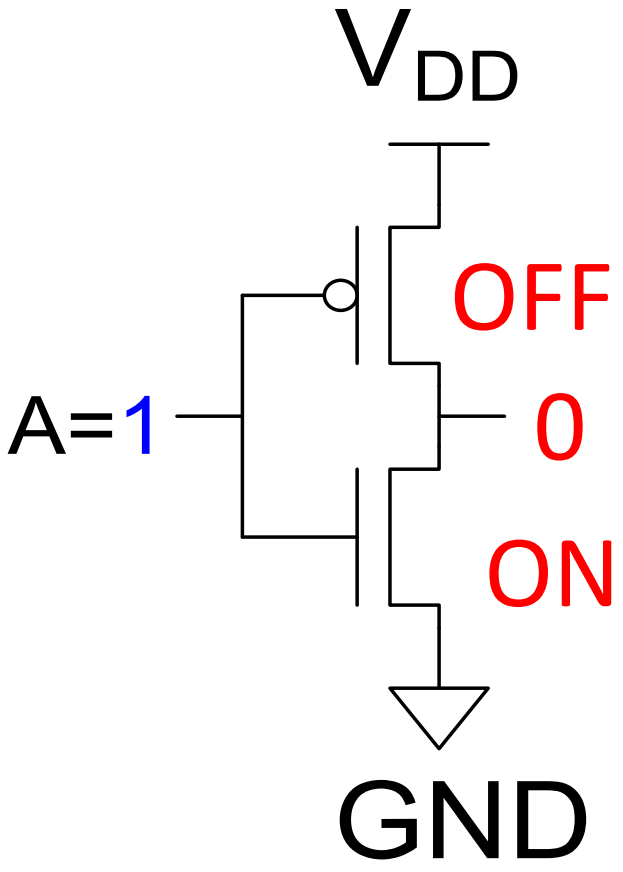
- Similar, but doping and voltages reversed
  - Input (V_G) at low voltage: transistor ON
  - Input (V_G) at high voltage: transistor OFF
  - Bubble indicates inverted behavior



CMOS Inverter

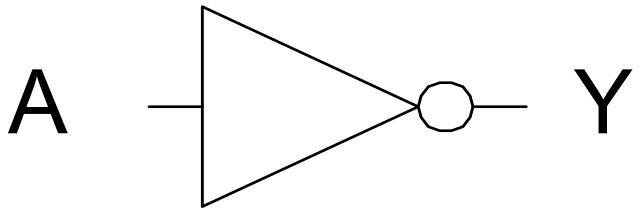
A	Y
0	
1	0

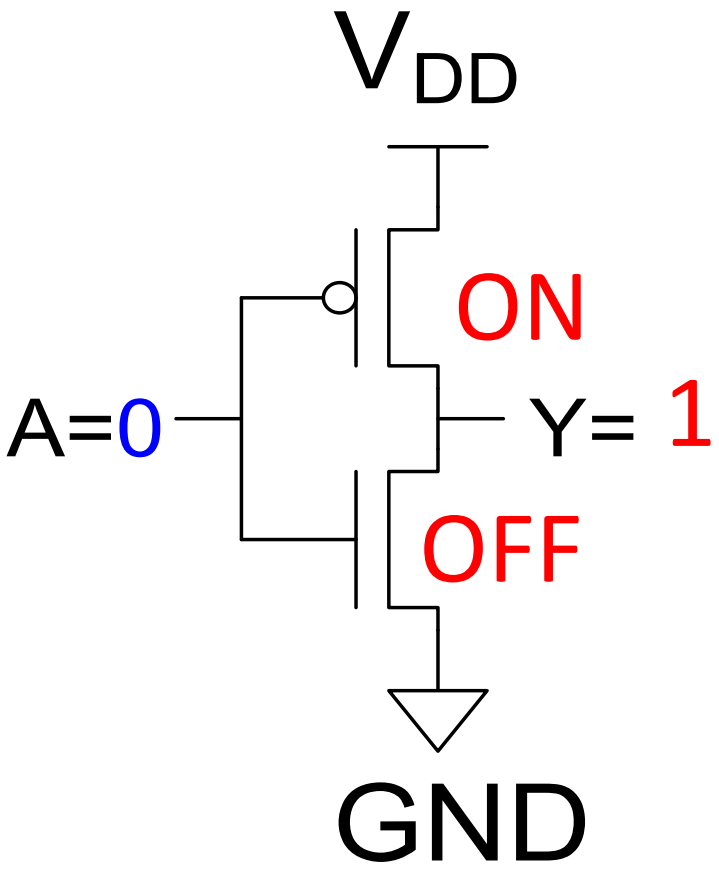




CMOS Inverter

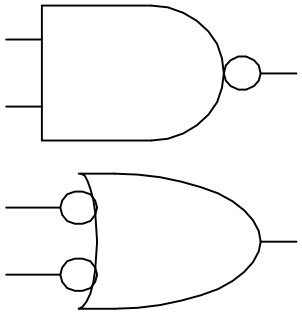
A	Y
0	**1**
1	0

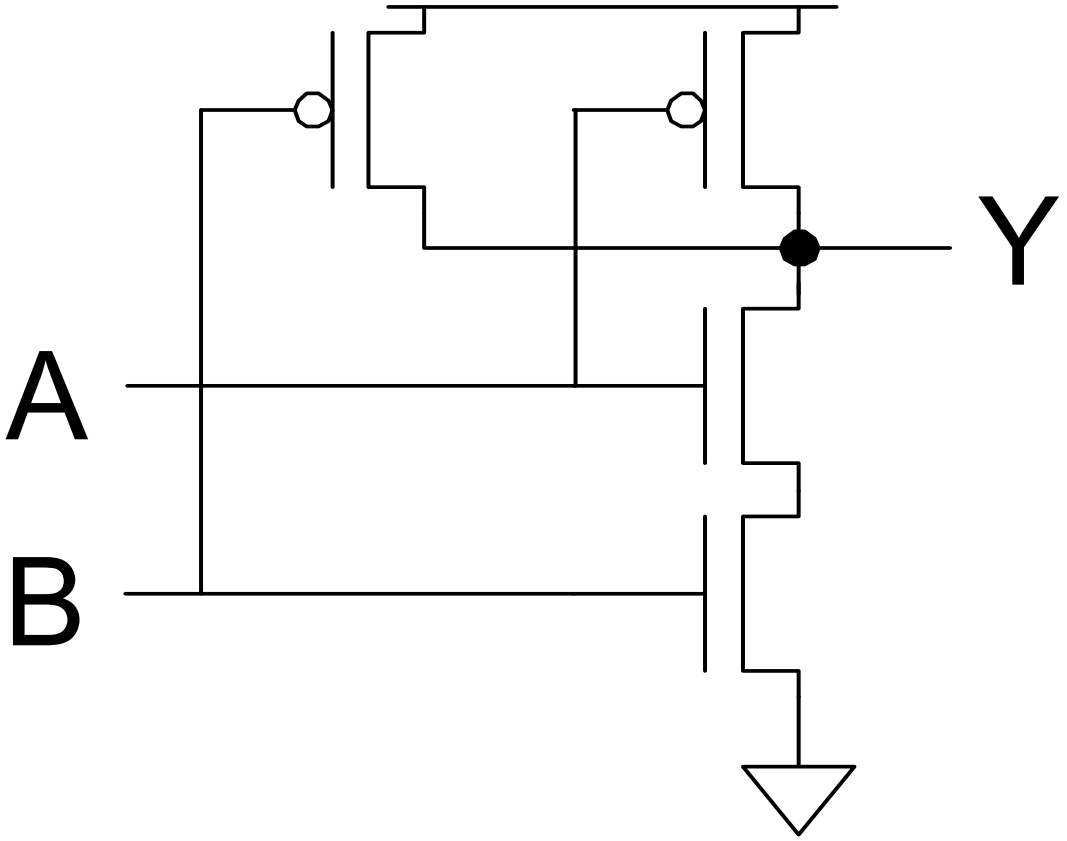




CMOS NAND Gate

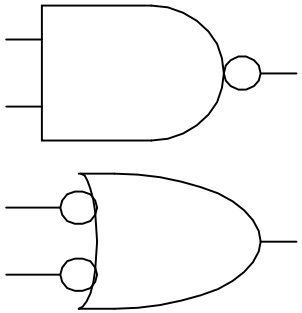
A	B	Y
0	0	
0	1	
1	0	
1	1	

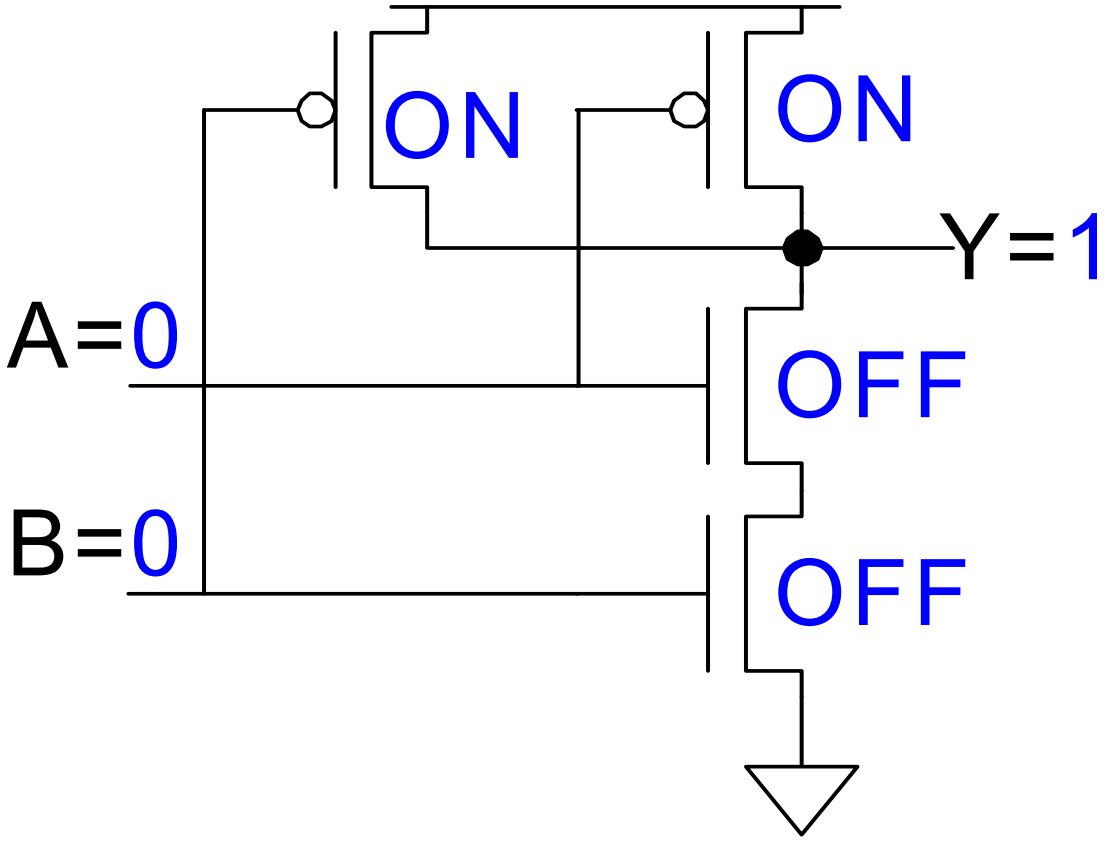




CMOS NAND Gate

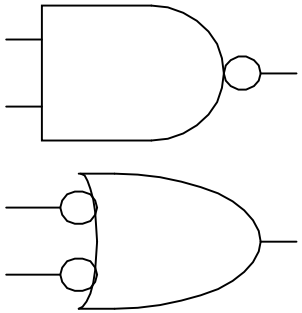
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

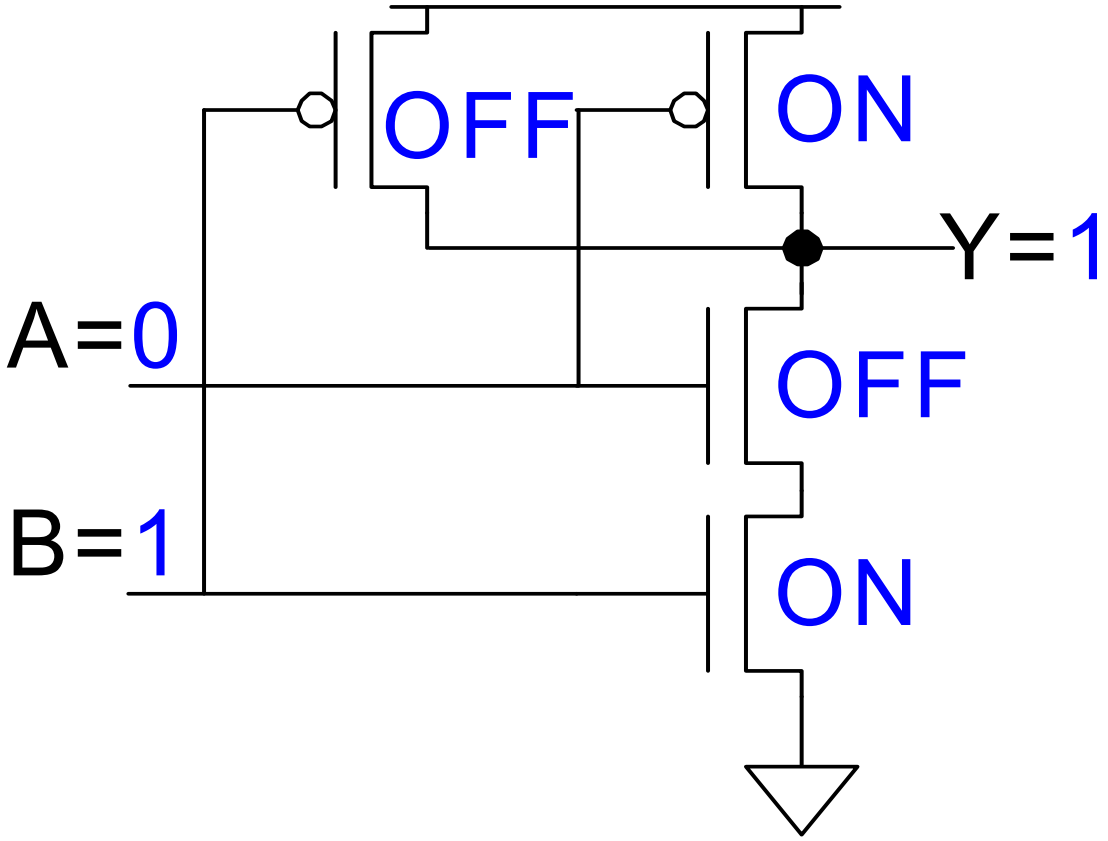




CMOS NAND Gate

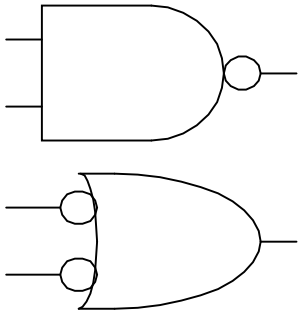
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

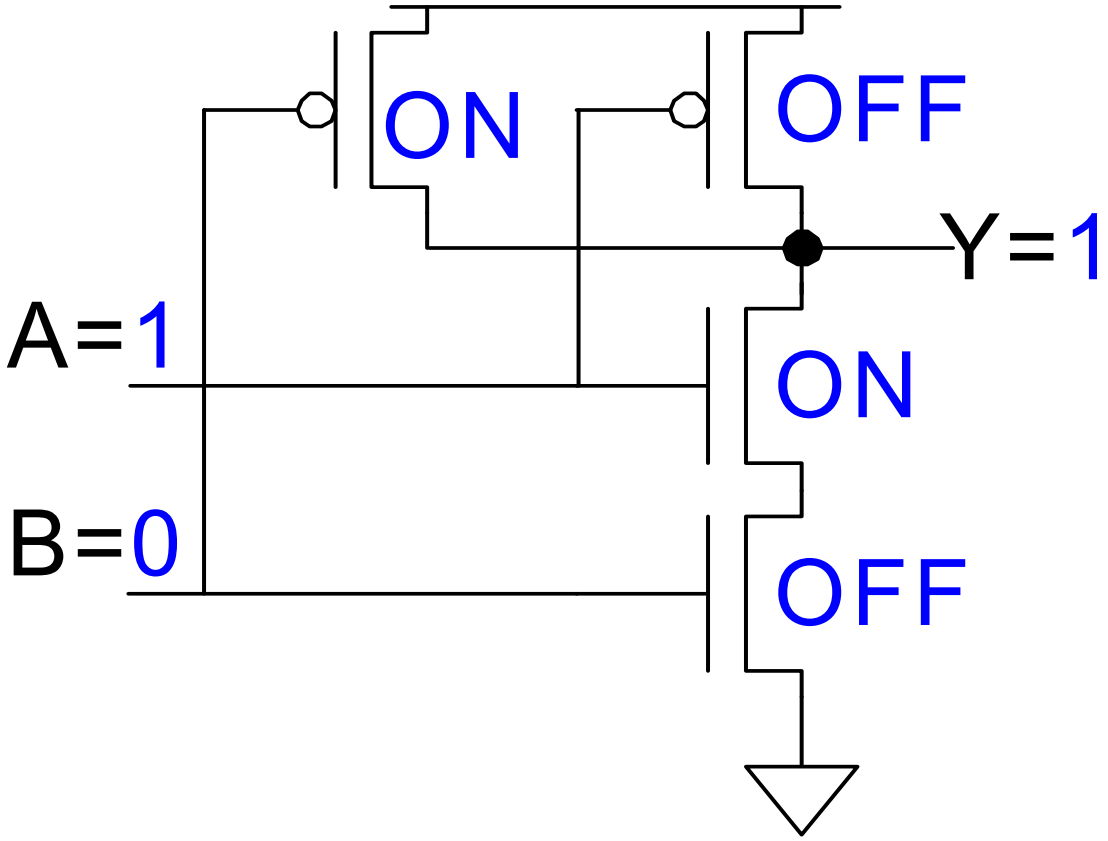




CMOS NAND Gate

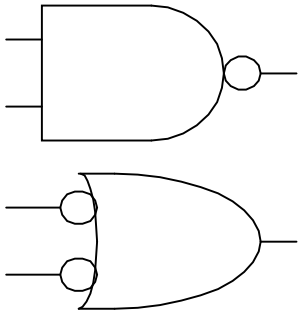
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

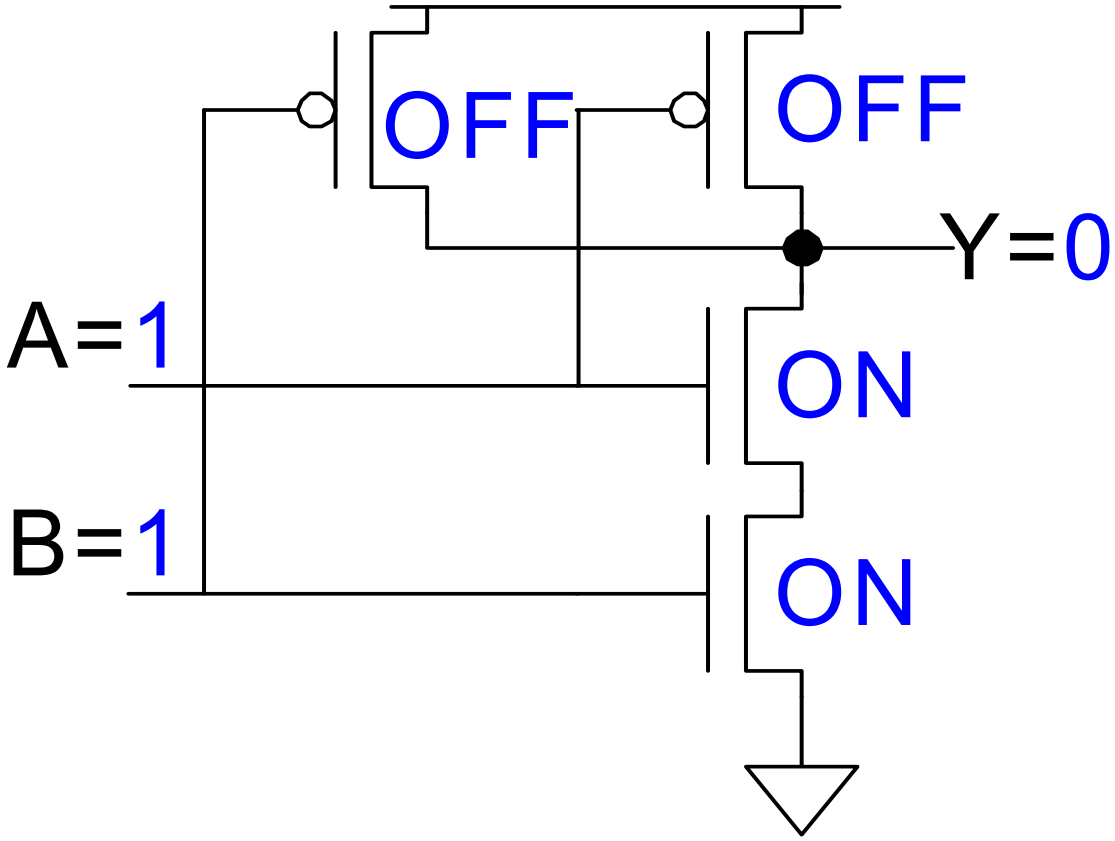




CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

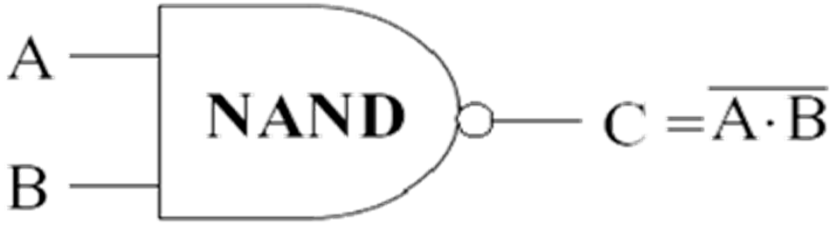


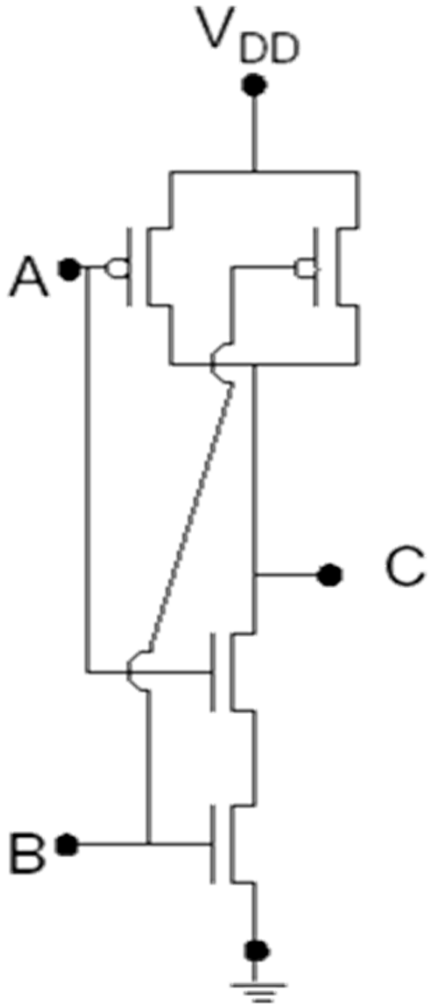


Use Switch to build Gates

- CMOS NAND:

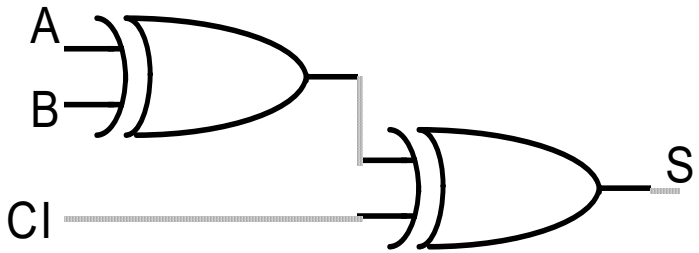
A	B	A B	C= $\overline{A\ B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

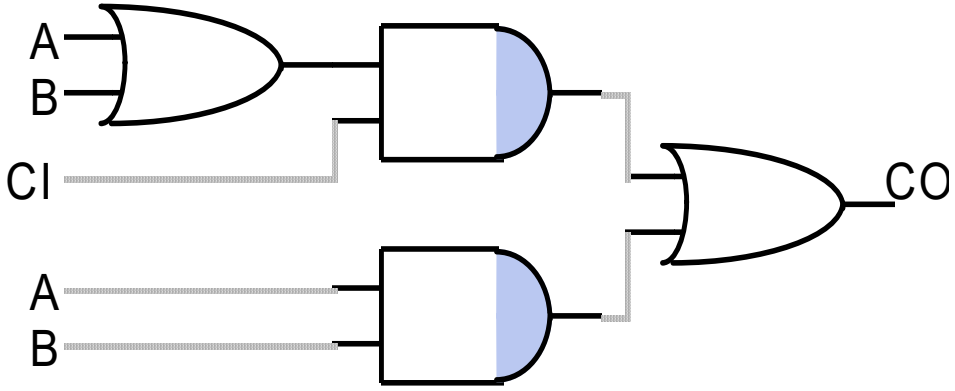




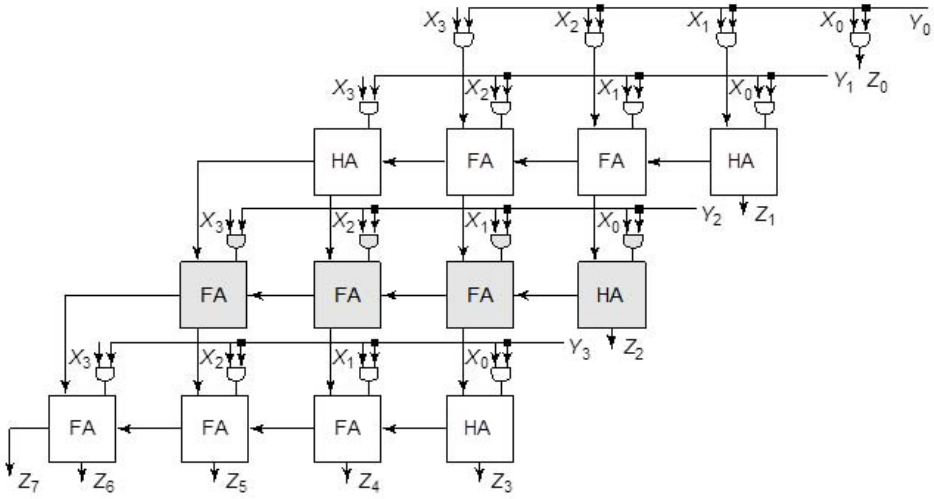
Use gates to build logic blocks

- Full Adder

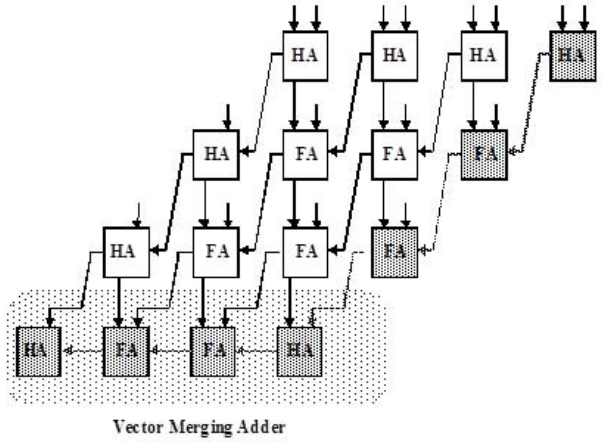




The Array Multiplier



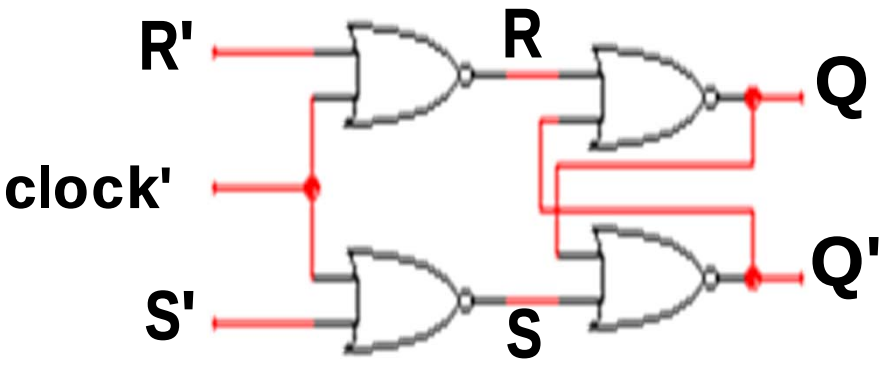
Carry-Save Multiplier



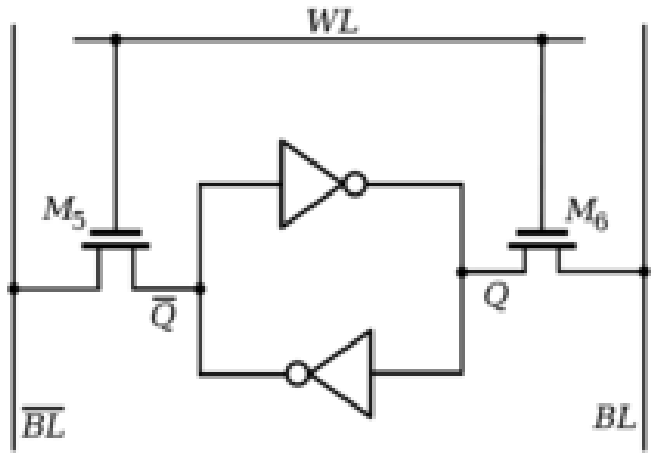
$$t_{mult} = (N-1)t_{carry} + (N-1)t_{and} + t_{merge}]$$

Use gates to build memory element

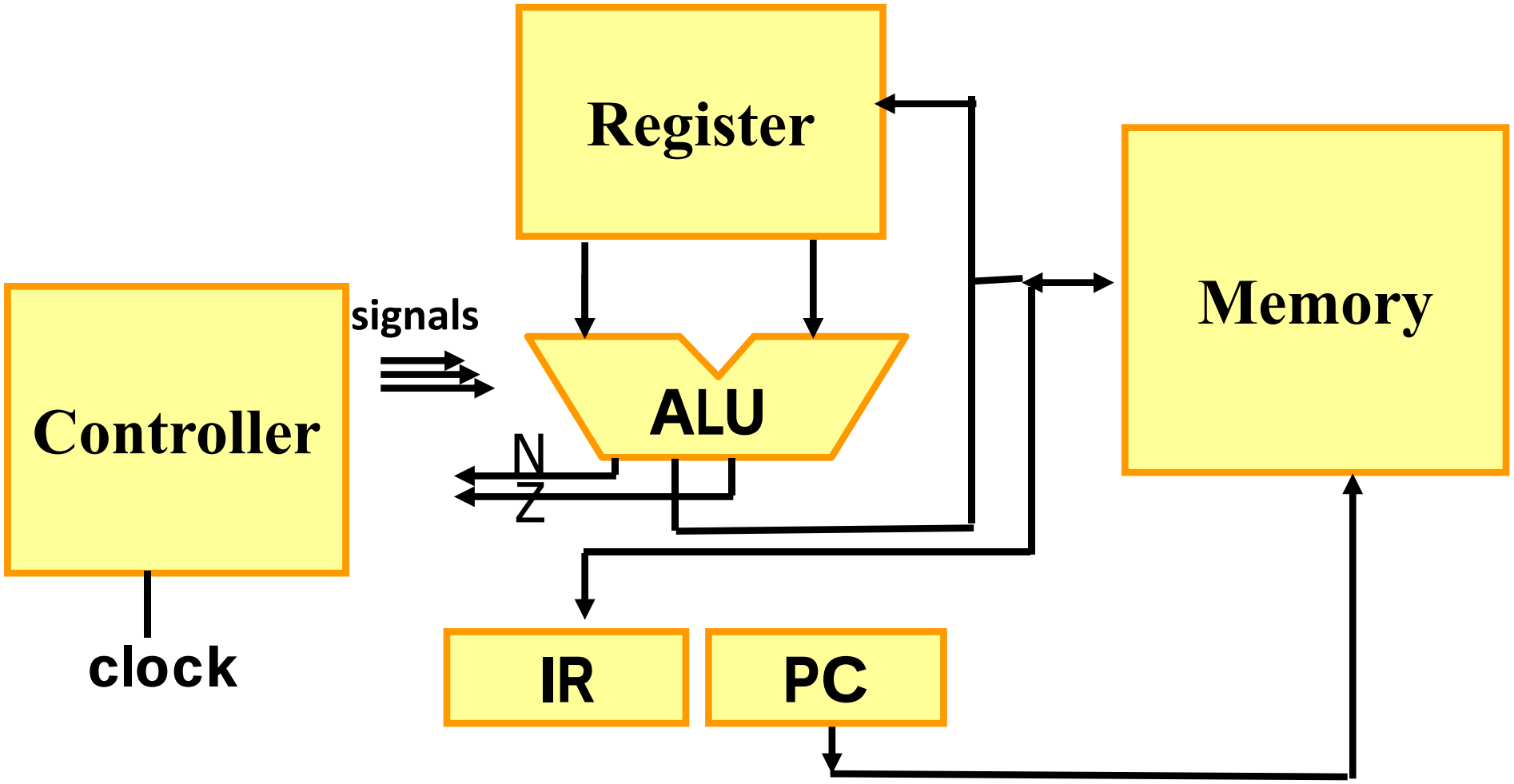
- Circuit to store 1-bit data
  - SR Latch



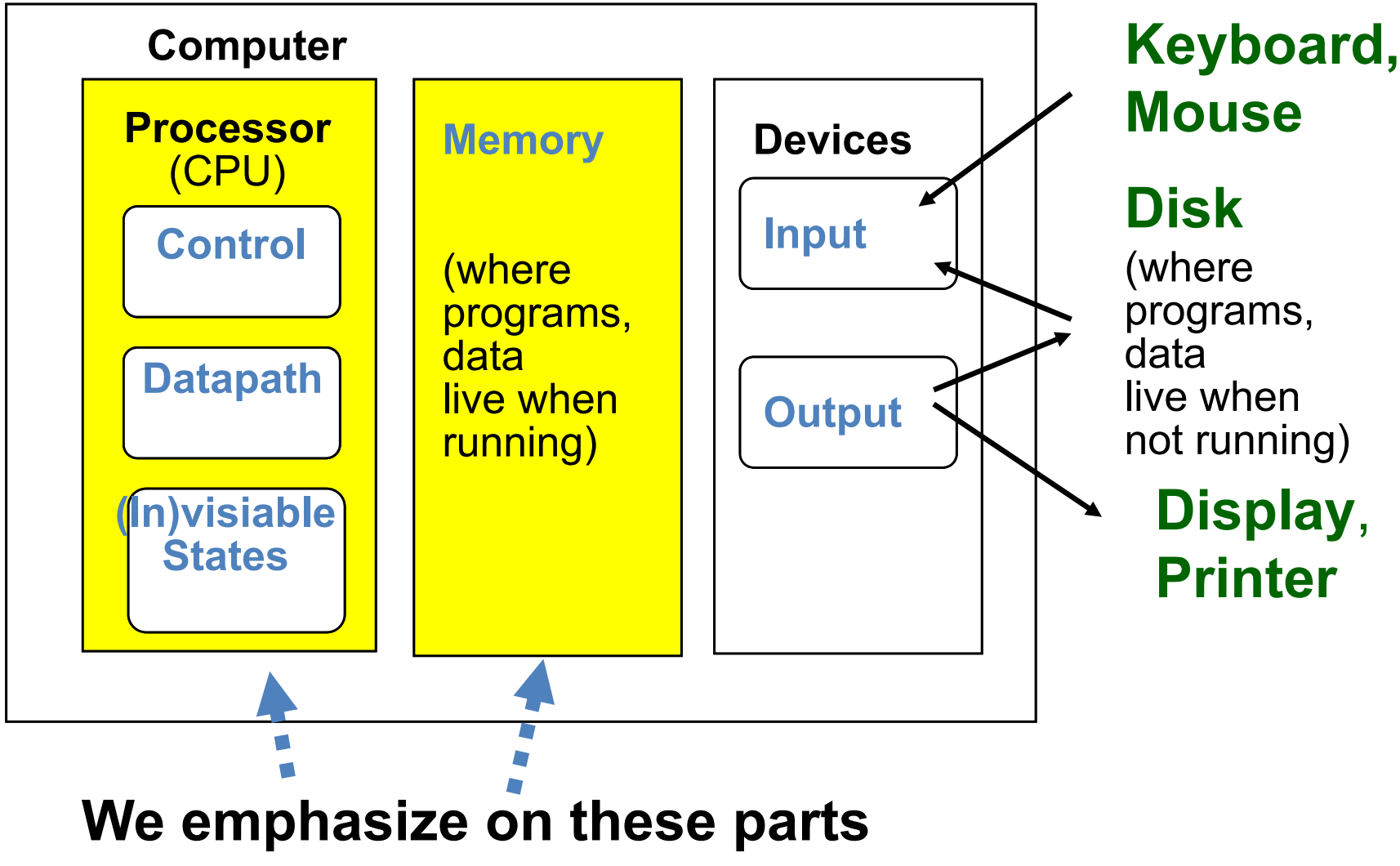
  - SRAM cell



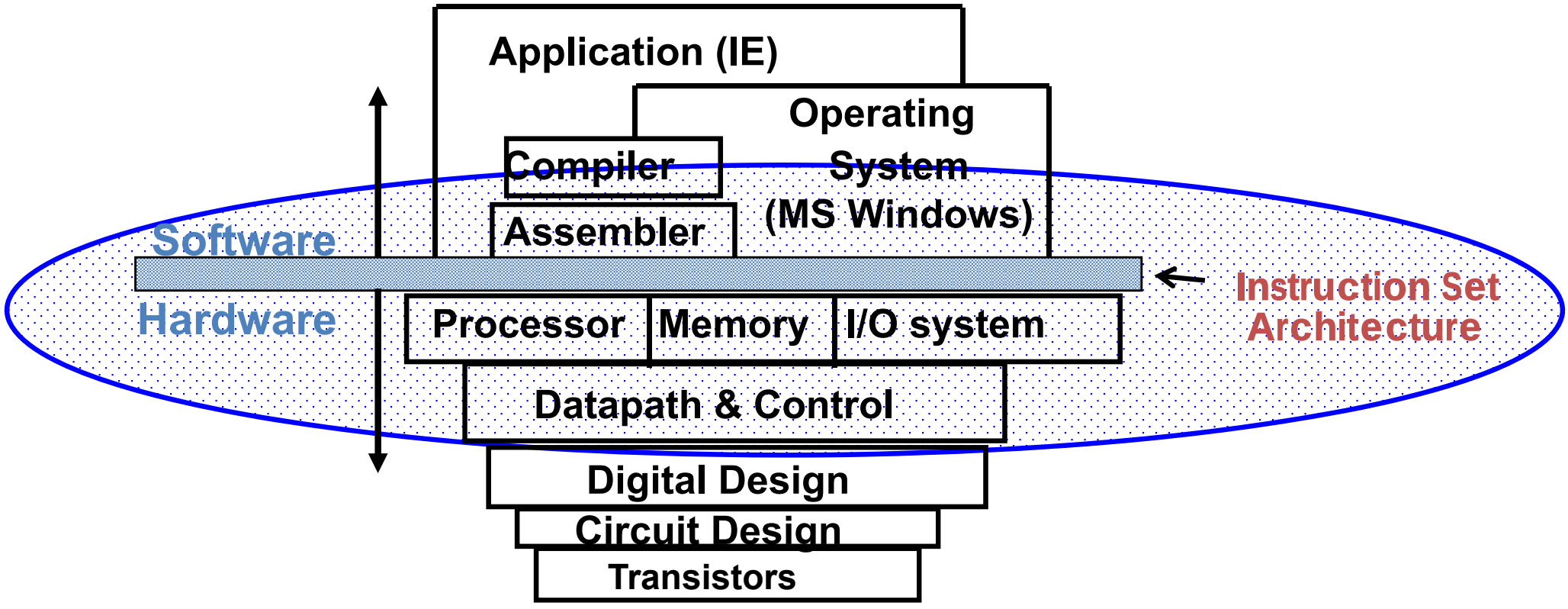
Use logic blocks to build a CPU



Basic Organization of a Computer

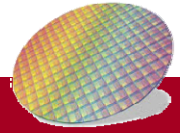


Computer Organization: Hardware/Software Interface



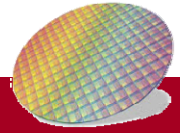
Thank you for your listening!

Any Questions?



Why We Learn Computer Organization?

- Required
- It impacts every other aspect of electrical engineering and computer science
- One of the foundations in computer science



Backup Slides